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[54] **INTEGRATED CIRCUIT PACKAGE WITH OVERLAPPED DIE ON A COMMON LEAD FRAME**

[75] **Inventor:** Carmen D. Burns, Austin, Tex.

[73] **Assignee:** Staktek Corporation, Austin, Tex.

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**Related U.S. Application Data**

[63] Continuation of Ser. No. 380,542, Jan. 30, 1995, abandoned.

[51] **Int. Cl.<sup>o</sup>** ..... H01L 23/50; H01L 23/10; H01L 27/10; H01L 23/28

[52] **U.S. Cl.** ..... 257/676; 257/792; 257/729; 257/686; 257/703; 257/700; 257/666; 257/699

[58] **Field of Search** ..... 257/466, 676, 257/686, 699, 700, 701, 702, 703, 708, 729, 792, 777, 723

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*Primary Examiner*—Sara W. Crane

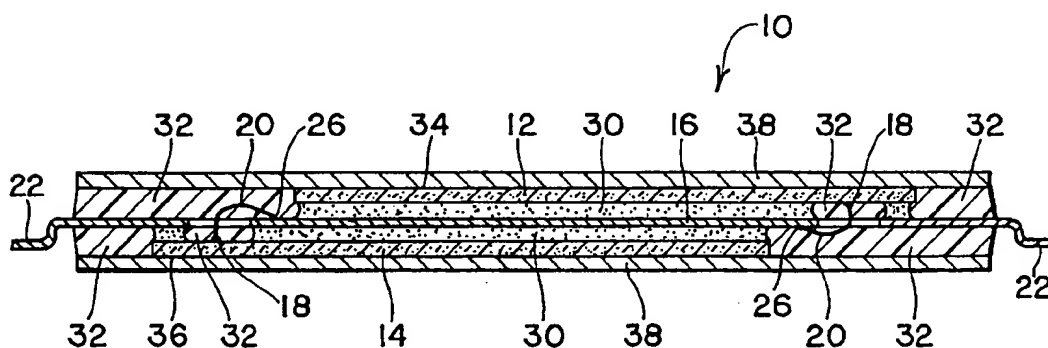
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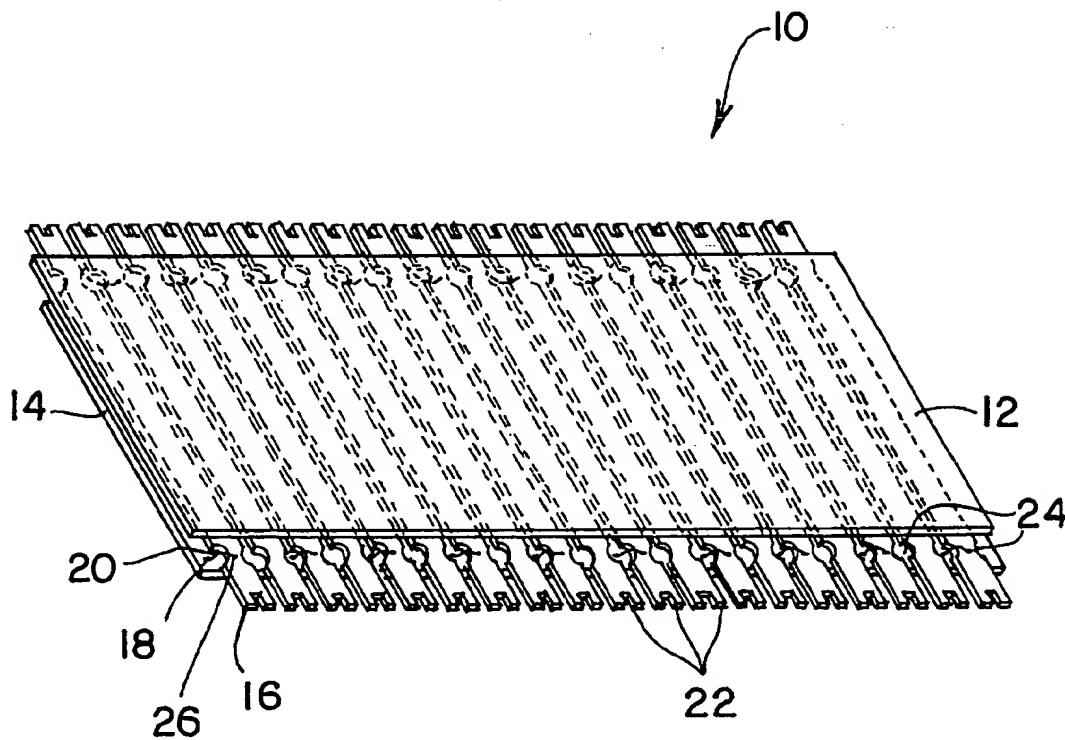
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[57] **ABSTRACT**

This invention is for an integrated circuit package which includes two integrated circuit die connected to a common substantially planar lead frame, wherein bond pads on each die face the common lead frame.

**19 Claims, 2 Drawing Sheets**



*FIG. 1*

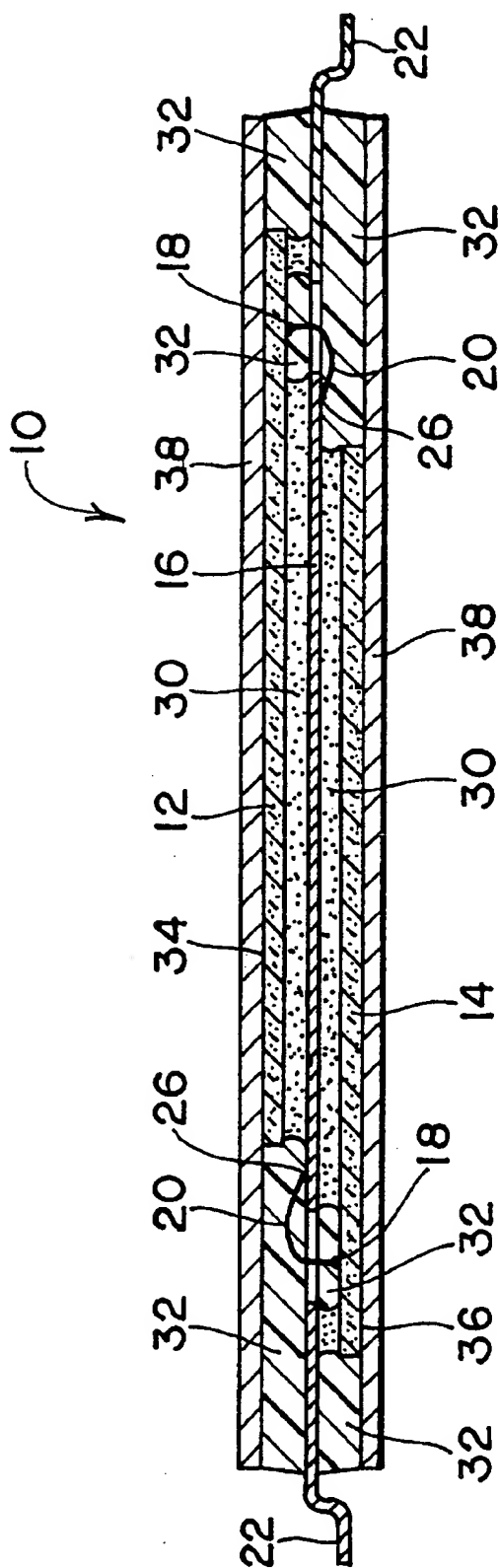


FIG. 2

# INTEGRATED CIRCUIT PACKAGE WITH OVERLAPPED DIE ON A COMMON LEAD FRAME

## CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a continuation of application Ser. No. 08/380,542, filed Jan. 30, 1995, now abandoned.

## BACKGROUND OF THE INVENTION

### 1. Field of the Invention

This invention relates to a high density integrated circuit package having a plurality of integrated circuit die attached to a common lead frame.

### 2. Discussion of the Related Technology

Modern microprocessor-based computer systems, including personal computers, require increased memory storage capability, with faster access which, nonetheless, use the same space on mother boards or other printed circuit boards as prior memory devices. Apparatus and methods for achieving a high density, three-dimensional integrated circuit memory package having a small footprint are described in U.S. Pat. No. 5,279,029, entitled, Ultra High Density IC Packages Method, and U.S. Pat. No. 5,367,766, also entitled Ultra High Density IC Packages Method, both assigned to the common assignee of the present invention.

These related patents describe an apparatus and method of manufacturing a three-dimensional high density integrated circuit module, which provides a plurality of individual integrated circuit packages stacked vertically without additional board space. In these ultra high density modules electrical leads extending from each of the individual integrated circuit packages in the module are electrically coupled to each other and to external circuitry via an external conductive rail assembly.

For flash memory applications, such as smart cards and the like, even greater memory density is required. That is, more memory in a low profile package is needed without increasing the footprint area of the device and without increasing the number of electrical leads extending from such a package.

## SUMMARY OF INVENTION

The present invention provides a low profile very high density integrated circuit memory device. The design of the present invention includes at least two integrated circuit die mounted with the active surfaces facing a common lead frame. The die and lead frame are contained within a protective casing. The design of the present invention can be used with any suitable integrated circuit dies, but is particularly well suited for use with high density flash memory devices. The packaging design of the present invention provides a higher density memory device without increasing the package profile, footprint or the total number of leads necessary for interconnection to external circuitry.

In the preferred embodiment, each die includes a single row of wire bond pads located on an outer edge of the active or signal surface of the die. The mounted die are slightly offset from one another so the single row of wire bond pads on each die are exposed and not overlaid by the other die to facilitate wire bonding to the lead frame. The bonding wires, which are attached to the wire bond pads on each die, are then connected to the common lead frame disposed between the two die by wire bonding, wedge bonding or thermal

compression bonding the end of each bonding wire to a bonding pad on the common lead frame. The common lead frame overlays a substantial portion of the surface of each die and is mounted to each die by a double-sided polyimide tape, or by a high-temperature adhesive or epoxy layer.

After the two die are mounted to the common lead frame, and the die wire bond pads attached by bond wires to the lead frame bonding pads, the die, lead frame and bonding wires are encased in a transfer molding material. The transfer molding is injected into a mold forming a protective casing which fills any voids in and around the die, the wire bond pads and the bond wires. This ensures the integrity of the wire bond connections. After molding, the upper and/or lower major surfaces of the casing are lapped to provide a thinner high density integrated circuit package. Metal foil may be laminated to the top and/or bottom of the lapped package to provide better thermal heat dissipation from the package.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a perspective view of a schematic representation of the connectivity of the double-die mounted to common lead frame configuration of the present invention; and

FIG. 2 is a cross-sectional view of the double-die configuration of the present invention.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

In FIG. 1, the double-die integrated circuit package 10 of the present invention is illustrated. An upper integrated circuit die 12 is laminated to a common lead frame 16. Common lead frame 16, preferably 3.0 mil thick copper, includes a plurality of individual substantially planar electrical conductors 22. A second integrated circuit die 14 is laminated to an opposite side of common lead frame 16.

As shown in FIG. 1, upper integrated circuit die 12 and lower integrated circuit die 14 are both mounted with their active surfaces, the surface which includes circuit interconnection wire bond pads 18, facing a common lead frame 16 and are slightly offset from each other so the wire bond pads 18 on each die are exposed and are easily accessible for wire bonding, wedging or wire compression bonding wires 20 to bonding pads 26 on each electrical conductor 22 of lead frame 16 during the manufacturing process. FIG. 1 schematically illustrates each integrated circuit die 12 and 14 which includes a single row of wire bond pads 18 disposed in a single column configuration along an outer edge of each die. It should be understood that wire bonds 18 may be arranged near an edge of each die in a non-linear configuration, such as a plurality of staggered rows, or otherwise. At a minimum, the wire bond pads 18 for each integrated circuit die 12 and 14 are located within an area near an outer edge of each die. The area of wire bond pads 18 for each die 12 or 14 is not overlaid by the other respective die when the two die 12 and 14 are mounted to common lead frame 16.

The electrical connectivity of package 10 between wire bond pads 18 and electrical conductors 22 of lead frame 16 illustrated in FIG. 1 does not necessarily represent the actual connectivity of package 10. FIG. 1 is merely illustrative of the general arrangement of the bond pads 18 and lead frame 16. The actual selective connectivity of package 10 is determined by: 1) the presence or absence of a wire bond pad 18 for each electrical conductor 22; 2) the pattern and layout of the electrical conductors 22 of lead frame 16, which may not all run parallel to each other as shown in FIG.

1; and/or 3) selectively connecting certain of the electrical conductors 22 to an external rail assembly, as described in commonly assigned U.S. Pat. Nos. 5,279,029 and 5,367,766, referenced previously.

Preferably, electrical conductors 22 include notches 24 which allow bonding wires 20 to be looped over and attached to bonding pads 26 on lead frame 16 more easily, since there is limited space between each electrical conductor 22. Attempting to loop bonding wires 20 without the notches 24 would be more difficult and time consuming. The electrical connections for upper integrated circuit die 12 between wire bond pads (not shown) on upper die 12 and lead frame 16 are schematically illustrated and are identical to the connections for lower die 14.

Preferably, several process steps are followed to create the double die integrated circuit package 10 of the present invention. Referring to FIG. 2, the upper integrated circuit die 12, or lower integrated circuit die 14, is first mounted to lead frame 16 using an adhesive layer 30, which is a high temperature non-conductive adhesive, such as polyimide tape, or a low shrink epoxy. After this step, the remaining unattached integrated circuit die is mounted to lead frame 16 using an adhesive layer 30. The bonding wires 20 of the two integrated circuit die 12 and 14 are then attached, via solder wedge bonding or thermal compression bonding, to wire bond pads 18 of each die. Bonding wires 20 are then soldered, wedge bonded or thermal compression bonded to bonding pads 26 of select electrical conductors 22 on common lead frame 16.

Once the two die 12 and 14 are mounted to common lead frame 16 and all electrical interconnections between the two die 12 and 14 and the common lead frame 16 are made, the assembly is inserted into a molding chamber, as described in U.S. Pat. No. 5,279,029, issued to Burns, entitled Ultra High Density IC Packages Method, which is incorporated herein in its entirety for all purposes. The double die and common lead frame assembly is then encased with an injected plastic transfer molding material 32. The transfer molding material 32 is injected so it fills in any voids in and around either die 12 or 14, the wire bond pads 18, the bonding wires 20 and bonding pads 26.

After hardening, package 10 is removed from the mold and both the upper and lower major surfaces, 34 and 36, of the package 10 are lapped until the desired thickness of the overall package 10 is achieved. Next, edges of package 10 are covered with a masking means, such as a rubber gripper, tape or liquid solder stop. The transfer molded material 32 and exposed silicon die 12 or 14 after lapping are then pretreated with a plating pretreatment. The unmasked areas of the package 10 are then electroless plated. An electrode is attached and the entire package 10 is electroplated with a very thin layer of copper, nickel or chrome, or any continuous metal layer, forming a light tight seal free of imperfections or pinholes. The masking is then removed and the integrated circuit package 10 of the present invention is achieved.

In another embodiment, after the upper and lower die 12 and 14 are mounted to the common lead frame 16 with adhesive layer 30, a layer of high temperature polymer, which is preferably a low shrink epoxy, such as ABLE-STICK brand B-staged epoxy, is injected between the upper die 12 and the common lead frame 16 and between the lower die 14 and the common lead frame 16 to fill all voids. The entire assembly is then compressed to squeeze together the layers to remove all voids, and is then heated to cure the injected epoxy.

In an alternative embodiment, after being encased by molding material 32, the upper and/or lower major outer surfaces 34 and 36 of the casing are lapped to provide a thin, high density integrated circuit package 10. A thin layer of metal foil 38 may be mounted to the top and/or bottom surface 34 and 36 of package 10 to provide better thermal heat dissipation from package 10.

The integrated circuit package 10 of the present invention is warp balanced, that is, the assembly which includes the two die 12, 14 and the common lead frame 16 disposed therebetween results in a warp resistant, zero warp structure due to the center line balance achieved with the two die 12, 14 being mounted one over another on a common lead frame 16. Because of this configuration, the die 12, 14 and common lead frame 16 assembly will remain essentially planar, since any warping forces on one die will be offset by warping forces of equal magnitude and opposite direction on the remaining die. Thus, a warp resistant, substantially planar package 10 is achieved.

The foregoing disclosure and description of the invention are illustrative and explanatory of the preferred embodiments, and changes in the individual components, elements or connections may be made without departing from the spirit of the invention and the scope of the following claims.

What is claimed is:

1. An integrated circuit package, comprising:

a first integrated circuit die, said first die having a plurality of circuit interconnection pads on a major surface of said first die;

a second integrated circuit die, said second die having a plurality of circuit interconnection pads on a major surface of said second die;

wherein said first die and said second die are substantially the same in size and the layout of said integrated circuit of each said die is substantially the same; and

a substantially planar lead frame comprised of a plurality of electrical conductor elements, wherein said major surfaces of said first die and said second die are mounted to opposite sides of said lead frame so as to position said plurality of circuit interconnection pads on each said die adjacent corresponding ones of said plurality of electrical conductor elements on said lead frame;

wherein said lead frame substantially overlays each of said integrated circuit die, and wherein an adhesive layer is disposed between each said die and said lead frame.

2. The package of claim 1, wherein said circuit interconnection pads on each said die are located within an area near an outer edge on each said respective die.

3. The package of claim 1, further comprising a casing substantially surrounding said first and second die and said lead frame.

4. The package of claim 1, wherein said circuit interconnection pads are disposed along an edge of a major surface of each said die.

5. The package of claim 1, wherein said adhesive layer comprises a double-sided polyimide tape.

6. The package of claim 1, wherein said lead frame overlays a substantial portion of each said die.

7. The package of claim 1, wherein said circuit interconnection pads on each said die are disposed in a single row along an edge of a major surface of each said die.

8. The package of claim 3, wherein said casing is transfer molded plastic.

9. The package of claim 1, wherein said adhesive layer comprises a high temperature polymer adhesive.

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10. The package of claim 1, wherein bonding wires are connected between each said circuit interconnection pad on each said die and said lead frame.

11. The package of claim 1, wherein said lead frame is 3.0 mils thick.

12. The package of claim 2, wherein said area on said first die is not overlaid by said second die.

13. The package of claim 1, wherein at least one said circuit interconnection pad on said first die and at least one said circuit interconnection pad on said second die are electrically connected to a common lead frame electrical conductor element.

14. The package of claim 3, further comprising a metal foil layer attached to at least one of the major surfaces of said package.

15. A high density integrated circuit package, comprising:  
a first integrated circuit die, wherein said first die includes a plurality of bonding pads disposed in close proximity to an edge of a major surface of said first die, wherein said first die is mounted to a first major surface of a lead frame and is electrically connected thereto; and wherein said lead frame comprises a plurality of substantially planar electrical conductors;

a second integrated circuit die, wherein said second die includes a plurality of bonding pads disposed in close proximity to an edge of a major surface of said second

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die, and wherein said second die is mounted to a second major surface of said lead frame and is electrically connected thereto

wherein said first die and said second die are substantially the same in size and the layout of said integrated circuit of each said die is substantially the same;

wherein said lead frame is substantially planar and overlays each said integrated circuit die, an adhesive layer disposed between said first die and said first major surface of said lead frame and between said second die and said second major surface of said lead frame; and a casing substantially surrounding said first die, said second die and said lead frame, wherein electrical leads extend through said casing.

16. The package of claim 15, wherein said adhesive layer is a high temperature polymer adhesive.

17. The package of claim 15, wherein said adhesive layer comprises a double-sided polyimide tape.

18. The package of claim 15, wherein said lead frame is 3.0 mils thick.

19. The package of claim 15, further comprising bonding wires connected between said bonding pads on said first die and said lead frame and between said bonding pads on said second die and said lead frame.

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